LISTING OF THE CLAIMS

A detailed listing of claims is presented below. Please amend currently amended claims as indicated below including substituting clean versions for pending claims with the same number. In addition, clean text versions of pending claims not being currently amended that are under examination are also presented. It is understood that any claim presented in a clean version below has not been changed relative to the immediate prior version.

1. (Original) A semiconductor memory device comprising an array of memory cells arranged in rows and columns, wherein said array of memory cells comprises:

a plurality of non-intersecting STI regions isolating a plurality of columns of memory cells;

a source column implanted with n-type dopants isolated between an adjoining pair of said plurality of non-intersecting STI regions, said source column coupled to a plurality of source lines that are coupled to a plurality of source regions in said array of memory cells; and

a source contact coupled to said source column for providing electrical coupling with said plurality of source regions, said source contact located along a row of drain contacts that are coupled to drain regions of a row of memory cells.

2. (Original) The semiconductor memory device as described in claim 1, wherein locating said source contact along said row of drain contacts enables the straight

formation of a word line intersecting said source column near said source contact.

3. (Original) The semiconductor memory device as described in claim 1, wherein said n-type dopants are taken from a group consisting of:

arsenic;

phosphorous; and

antimony.

4. (Original) The semiconductor memory device as described in claim 1, further comprising:

a second source contact strapped to said source column for reducing resistance in said plurality of source lines, and located along a second row of drain contacts that are coupled to drain regions of a second row of memory cells.

5. (Original) The semiconductor memory device as described in claim 1, wherein each of said plurality of source lines is a common source line.

6. (Original) The semiconductor memory device as described in claim 1, further comprising:

a second source column implanted with said n-type dopants and isolated between a second adjoining pair of said plurality of non-intersecting STI regions, said source column coupled to said plurality of common source lines, said source column located x columns of memory cells from said source column in claim 1 for reducing resistance in said plurality of common source lines.

7. (Original) The semiconductor memory device as described in claim 6, wherein said x is the number 16.

8. (Original) A non-volatile semiconductor memory device including an array of memory cells, said array of memory cells comprising:

a source column implanted with n-type dopants, said source column coupled to a plurality of common source lines that are coupled to a plurality of source regions of memory cells in said array of memory cells, said source column arranged perpendicular to each of said plurality of common source lines; and

a source contact coupled to said source column for providing electrical coupling with said plurality of source regions, said source contact located along a row of drain contacts coupled to drain regions of a row of memory cells that are arranged perpendicular to said source column.

9. (Original) The non-volatile semiconductor memory device as described in claim 8, further comprising:

a plurality of word lines coupled to control gate regions of memory cells in said array of memory cells, said plurality of word lines exhibiting straightness at intersections with said source column adjacent to said source contact.

10. (Original) The non-volatile semiconductor memory device as described in claim 8, further comprising:

a plurality of STI regions arranged in non-intersecting columns on a silicon substrate, said plurality of STI regions isolating columns of memory cells in said array of memory cells, and isolating said source column.

11. (Original) The non-volatile semiconductor memory device as described in claim 8, wherein said source contact is of similar dimension as each of said row of drain contacts.

12. (Original) The semiconductor memory device as described in claim 8, wherein memory cells in said array of memory cells are arranged in a NOR configuration.

13. (Original) The semiconductor memory device as described in claim 8, wherein at least one of said array of memory cells is a flash memory cell comprising:

a tunnel oxide layer formed on a semiconductor substrate between source and drain regions;

a floating gate formed on said tunnel oxide layer;

a multi-level insulating layer formed on said floating gate; and

a control gate formed on said insulating layer.

14. (Original) The semiconductor memory device as described in claim 8, further comprising

a second source contact strapped to said source column for reducing resistance in said plurality of common source lines, and located along a second row of drain contacts that are coupled to drain regions of a second row of memory cells.

15. (Original) The semiconductor memory device as described in claim 8, further comprising:

a second source column implanted with said n-type dopants, said source column coupled to said plurality of

common source lines, said source column located x columns of memory cells from said source column in claim 1 for reducing resistance in said plurality of common source lines.

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